

CLAIM AMENDMENTS

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided. The status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

Claims 1 - 27 (**Canceled**).

1 28. (**Currently Amended**): A semiconductor memory cell including at least one
2 transistor to constitute the memory cell, the at least one transistor of the memory cell
3 comprising:
4 a source region;
5 a drain region;
6 a body region disposed between the source region and the drain region, wherein
7 the body region is electrically floating; and
8 a gate disposed over the body region; and
9 wherein the memory cell includes:
10 a first data state representative of a first charge in the body region; and
11 a second data state representative of a second charge in the body region
12 wherein the second charge is substantially provided by removing charge from the
13 body region through the source region.

1 29. (**Previously Presented**): The memory cell of claim 28 wherein the first
2 charge is comprised of an accumulation of majority carriers in the body region.

1 **30. (Previously Presented):** The memory cell of claim 29 wherein the body
2 region is comprised of a P-type semiconductor material and the source and drain
3 regions are comprised of an N-type semiconductor material.

1 **31. (Previously Presented):** The memory cell of claim 29 wherein the majority
2 carriers accumulate in a portion of the body region that is adjacent to the source region.

1 **32. (Previously Presented):** The memory cell of claim 28 wherein positive
2 voltages are applied to the drain region and the gate to provide the second charge in
3 the body region.

1 **33. (Previously Presented):** The memory cell of claim 28 wherein positive
2 voltages are applied to the drain region and the gate to remove at least the first charge
3 from the body region.

1 **34. (Previously Presented):** The memory cell of claim 33 wherein, in response
2 to positive voltages being applied to the drain region and the gate, the transistor of the
3 memory cell includes a junction between the body region and the source region,
4 wherein the junction is forwarded biased.

1 **35. (Previously Presented):** The memory cell of claim 33 wherein, in response
2 to the positive voltages being applied to the drain region and the gate, the transistor of

3 the memory cell includes a forward bias current between the body region and the
4 source region.

1 36. **(Previously Presented):** The memory cell of claim 33 wherein the second
2 charge is stored in the body region in response to removing the positive voltages from
3 the drain region and the gate.

1 37. **(Currently Amended):** A semiconductor memory cell including at least one
2 transistor to constitute the memory cell, the at least one transistor of the memory cell
3 comprising:

4 a source region having impurities to provide a first conductivity type;

5 a drain region having impurities to provide the first conductivity type;

6 a body region disposed between the source region and the drain region wherein
7 the body region is electrically floating and includes impurities to provide a second
8 conductivity type wherein the second conductivity type is different from the first
9 conductivity type;

10 a gate disposed over the body region;

11 wherein the memory cell includes:

12 a first data state representative of a first charge in the body region wherein
13 the first charge is substantially provided by impact ionization; and

14 a second data state representative of a second charge in the body region
15 wherein the second charge is substantially provided by removing charge from the
16 body region through the source region.

1 **38. (Previously Presented):** The memory cell of claim 37 wherein the first
2 charge is comprised of majority carriers and wherein the second conductivity type is a
3 P-type.

1 **39. (Previously Presented):** The memory cell of claim 37 wherein, in response
2 to a first positive voltage applied to the drain region and a second positive voltage
3 applied to the gate, at least the first charge is removed from the body region through the
4 source region.

1 **40. (Previously Presented):** The memory cell of claim 39 wherein the memory
2 cell, in response to the first and second positive voltages, includes a junction between
3 the body region and the source region which is forwarded biased.

1 **41. (Previously Presented):** The memory cell of claim 40 wherein the first
2 conductivity type is an N-type.

1 **42. (Previously Presented):** The memory cell of claim 41 wherein the second
2 charge is stored in the body region in response to removing the first positive voltage
3 from the drain region before removing the second positive voltage from the gate.

1 **43. (Previously Presented):** The memory cell of claim 41 wherein, in response
2 to the first and second positive voltages, the transistor includes a forward bias current
3 between the body region and the source region.

1 **44. (Previously Presented):** The memory cell of claim 43 wherein the second
2 charge is stored in the body region in response to removing the first positive voltage
3 from the drain region and the second positive voltage from the gate.

1 **45. (Previously Presented):** The memory cell of claim 37 wherein the first
2 charge is stored in the body region in response to applying a first negative voltage to the
3 drain region and a second negative voltage to the gate.

1 **46. (Previously Presented):** The memory cell of claim 45 wherein the transistor
2 of the memory cell stores the first charge in a portion of the body region that is adjacent
3 to the source region.

1 **47. (Currently Amended):** A semiconductor memory cell including at least one
2 transistor to constitute the memory cell, the at least one transistor of the memory cell
3 comprising:

4 a source region having impurities to provide a first conductivity type;

5 a drain region having impurities to provide the first conductivity type;

6 a body region disposed between the source region and the drain region wherein
7 the body region is electrically floating and includes impurities to provide a second
8 conductivity type wherein the second conductivity type is different from the first
9 conductivity type;

10 a gate spaced apart from, and capacitively coupled to, the body region;

11 wherein the memory cell includes:

12 a first data state representative of a first charge in the body region; and

13 a second data state representative of a second charge in the body region
14 wherein the second charge is substantially provided by removing charge from the
15 body region through the source region.

1 48. (Previously Presented): The memory cell of claim 47 wherein, in response
2 to a first voltage applied to the drain region and a second voltage applied to the gate,
3 the first charge is removed from the body region through the source region.

1 49. (Previously Presented): The memory cell of claim 48 wherein, in response
2 to removing the first voltage from the drain region before removing the second voltage
3 from the gate, the second charge is stored in the body region.

1 50. (Previously Presented): The memory cell of claim 48 wherein the second
2 charge is stored in the body region in response to applying ground to the drain region
3 before removing the second voltage from the gate.

1 51. (Previously Presented): The memory cell of claim 48 wherein the first
2 voltage and the second voltage are positive voltages which, during operation, are
3 applied for a finite duration.

1 52. (Previously Presented): The memory cell of claim 48 wherein the
2 transistor, in response to the first voltage and the second voltage, includes a junction
3 between the body region and the source region which is forward biased.

1 53. **(Previously Presented):** The memory cell of claim 52 wherein the first
2 voltage and the second voltage are positive voltages which are applied for a finite
3 duration.

1 54. **(Previously Presented):** The memory cell of claim 53 wherein, in response
2 to the positive voltages being applied to the drain region and the gate, the transistor
3 includes a forward bias current between the body region and the source region.

1 55. **(Previously Presented):** The memory cell of claim 54 wherein the transistor
2 stores the second charge in the body region in response to a third voltage being applied
3 to the drain region before a fourth voltage is applied to the gate.

1 56. **(Previously Presented):** The memory cell of claim 55 wherein the third and
2 fourth voltages are ground.

1 57. **(Previously Presented):** The memory cell of claim 48 wherein the transistor
2 stores the first charge in a portion of the body region that is adjacent to the source
3 region.

1 58. **(Previously Presented):** The memory cell of claim 57 wherein the first
2 charge is substantially provided by impact ionization.

1 59. **(Previously Presented):** The memory cell of claim 48 wherein, in response
2 to a first positive voltage applied to the drain region and a second positive voltage
3 applied to the gate, more than the first charge is removed from the body region through
4 the source region.

1 60. **(Previously Presented):** The memory cell of claim 59 wherein the first
2 positive voltage is less than the second positive voltage.